Article

A Novel Linear-Based Closed-Loop Control and Analysis of Solid-State Transformer

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Abstract: In this paper, a new linear-based closed-loop control method for a Solid-State Transformer (SST) has been proposed. In this new control method, individual current and voltage loops for each of the power conversion stages (AC-DC, DC-DC, DC-AC) are implemented. The feedback between the input and output control signals for each loop is achieved through the voltage on the DC link capacitors and the current transferred between the converters. This enables the SST to be controlled easily in a linear-based closed-loop manner without the need for complex computations. In order to evaluate the performance analysis of the proposed control system, a simulation of an SST with approximately 10 kVA apparent power was performed. Based on the obtained simulation results, the response time of the proposed control method for dynamic load variations was proved to be in the range of 40 milliseconds, and it has been observed that this method allows electrical power to be transferred from the load to the grid. The power factor value of SST under inductive load is measured to be approximately 99%, and the overall system efficiency is 96% and above, indicating that this proposed new control method has very high performance.

Keywords: solid-state transformer; high-frequency transformer; grid-connected power flow; power factor correction

1. Introduction

In recent years, progress in power electronics technologies has led to a significant advancement in high-power applications, for which power converter circuits are widely preferred. The most prominent high-power applications are Electrical Power Systems (EPS) and Renewable Energy Systems (RES), where converter circuits are used extensively [1]. EPS fundamentally consists of three main components, namely the generation, transmission, and distribution of electrical energy. High-power converters are used in the transmission and distribution areas, such as Unified Power Flow Controller (UPFC) [2], Static Var Compensator (SVC) [3], Static Synchronous Compensator (STATCOM) [4], and High Voltage Direct Current (HVDC) [5]. The electrical power generated in EPS improves in quality with the use of high-power converters, making these systems more reliable and controllable at any moment.

In order to lower the losses and increase the efficiency of transmission lines, AC voltage is mainly stepped up at the input stage of the transmission line and stepped down at distribution and consumption points as required. By stepping up the AC line voltage, the transmission line current will be proportionally decreased so that the ohmic losses, corresponding to conduction losses of the transmission line, which is proportional to the square of the RMS current, could be lowered. Exactly for this reason, in EPS, conventional power transformers (CPTs) are used to step up and step down AC grid voltage, but their operating frequencies are limited to 50/60 Hz.

Although CPTs are a vital component of EPS, they tend to be relatively inefficient in modern applications, particularly in smart grid systems where real-time dynamic mon-

itoring and control of power are essential [6]. Another disadvantage of CPTs is that any undesirable situation, such as voltage sag, fault current, harmonics, etc., on the primary/grid side is transferred to the secondary/load side. Finally, CPTs lack the power factor correction (PFC) feature [7].

Solid-State Transformers (SSTs), also known as electronic transformers, intelligent transformers, or universal transformers, have been proposed to overcome the disadvantages of CPTs. It performs AC-AC voltage conversion like CPTs but includes various power converters and high-frequency transformers (HFTs). Because SST performs power conversion at high frequencies using HFT, its size and weight are significantly reduced compared to an equivalent-power CPT. The first concept design of SST is given in Figure 1 [8,9].
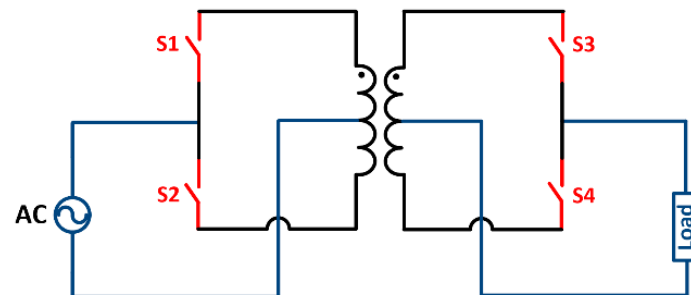

Figure 1. Concept design of SST.

In Figure 1, power transfer from the primary side to the secondary side occurs at high frequencies due to the direct application of a high-frequency and modulated AC voltage to the primary windings of an HFT resulting from the high-frequency operation of the switches. The concept-designed circuit, being the simplest version of the SST with a minimal number of semiconductor switches, operated at a lower voltage level initially due to constraints in semiconductor switch technologies during that time [10–12].

Depending on the power conversion stages, there are various SST topologies available. These are categorized as Types A, B, C, and D. Type A topology provides single-stage power conversion, while Types B and C involve systems with two-stage power conversion. Type D topology, on the other hand, offers three-stage power conversion, distinguishing it from the other topologies. Among these topology types, the most advantageous is Type D, which provides superior features in SST, such as power factor correction, high and low DC bus capability, bidirectional power flow, and grid integration. Therefore, in this study, the Type D topology, capable of three-stage power conversion, is preferred for the SST [7].

Today, all D-type prototypes produced operate in accordance with the working principle detailed in Figure 2. In this sense, the general operating criteria of a typical SST can be summarized as follows. Initially, low-frequency single/three-phase AC voltage is rectified with a rectifier stage followed by a DC-DC converter stage, which converts DC input voltage to high-frequency square wave AC voltage and applies to the primary winding of an HFT. High-frequency square wave AC voltage obtained at the secondary winding of the HFT is applied to a rectifier circuit at the secondary side of the DC-DC converter stage. Finally, rectified DC voltage is converted back to a low-frequency single/three-phase AC voltage by an inverter stage at the output of the SST. Due to the utilization of HFT for power conversion and isolation at high frequencies, the SST exhibits significantly reduced volume and weight compared to CPTs [13].

Various control methods have been proposed for SSTs, with Direct Feed Forward and Energy Feed Forward control methods being among them. Although both methods offer fast dynamic response times, they require a high computational load and may not achieve the desired performance under variable load conditions [14]. Another control method used in SSTs is the Model Predicted Direct Control, which enables direct power control and thereby enhances operational stability. Moreover, this method significantly reduces

harmonic distortion levels. However, its complex mathematical model poses challenges during implementation [15,16].
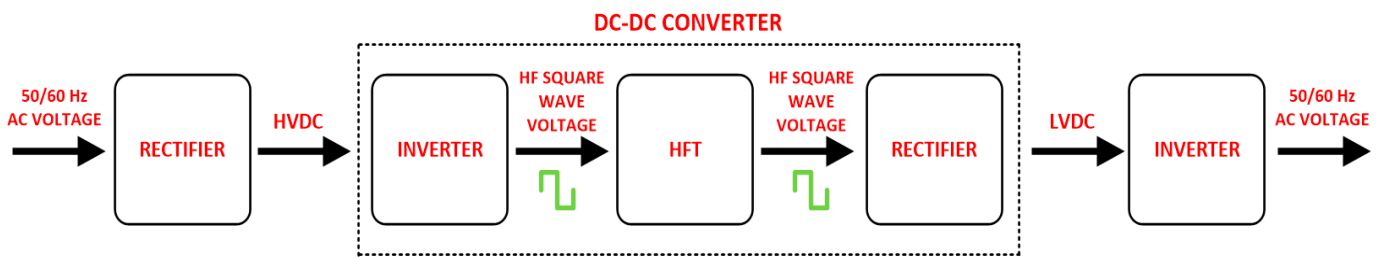

Figure 2. Working principle of SST.

It should be noted that the control methods proposed for SST have a complex mathematical model and heavy computational load depending on the topological structure of SST. This adversely affects system stability and can lead to undesirable performance outcomes. As a solution to the disadvantages of the control methods mentioned above, a new linear-based closed-loop control method has been proposed for SST systems capable of three-stage power conversion. This method designs individual current and voltage loops for each topology within the SST, regulating currents transferred between topologies and measuring voltages across DC link capacitors. As a result, a straightforward feedback mechanism is established, eliminating the need for high-computation control solutions.

Within the framework of this research, the topological structure of a 10 kVA SST has been examined, leading to the development of a mathematical model, and a new linear-based closed-loop control method has been proposed for the SST. The outline of the paper is as follows: in Section 2, the general circuit topology, mathematical model, and control structure of SST have been examined. In Section 3, the details of the proposed linear-based closed-loop control method are explained. Finally, in Section 4, the simulation of the proposed control method has been performed, and the results have been evaluated.

2. Topological Structure of SST

A typical SST structure consists of three converter power stages with a cascade connection via a DC link capacitor. These power stages are a three-phase Active Front-End (AFE) AC-DC Converter, Dual Active Bridge (DAB) DC-DC converter and three-phase DC-AC inverter, respectively. The general topological structure of SST with each circuit is given in Figure 3.
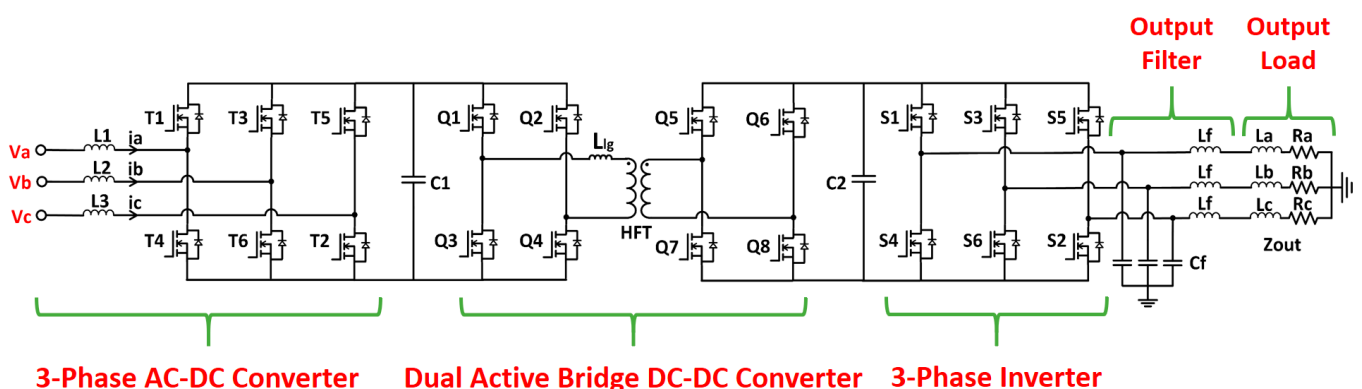

Figure 3. Topological structure of SST.

Since power semiconductor switches such as IGBTs or MOSFETs are utilized in the SST structure, closed-loop control with good dynamic response along with bidirectional power flow could be adapted. The aforementioned power stages utilized in SST have been comprehensively analyzed in upcoming sections.

2.1. Three-Phase Active Front-End AC-DC Converter

The three-phase AC-DC converter circuit, shown in Figure 3, is operated as an active front-end to stabilize the DC link bus voltage by generating control pulses with the Space Vector Pulse Width Modulation (SVPWM) technique in a closed-loop control manner [17,18]. By increasing the switching frequency within the limit values, it is possible to reduce the Total Harmonic Distortion (THD) of the input current in an AFE converter controlled by SVPWM. Additionally, by using SVPWM, the pulse width times of the switches are modulated very quickly in real time, thus providing PFC under ohmic-inductive load conditions. The control structure of the AFE consists of voltage and current control loops, which are illustrated in Figure 4.
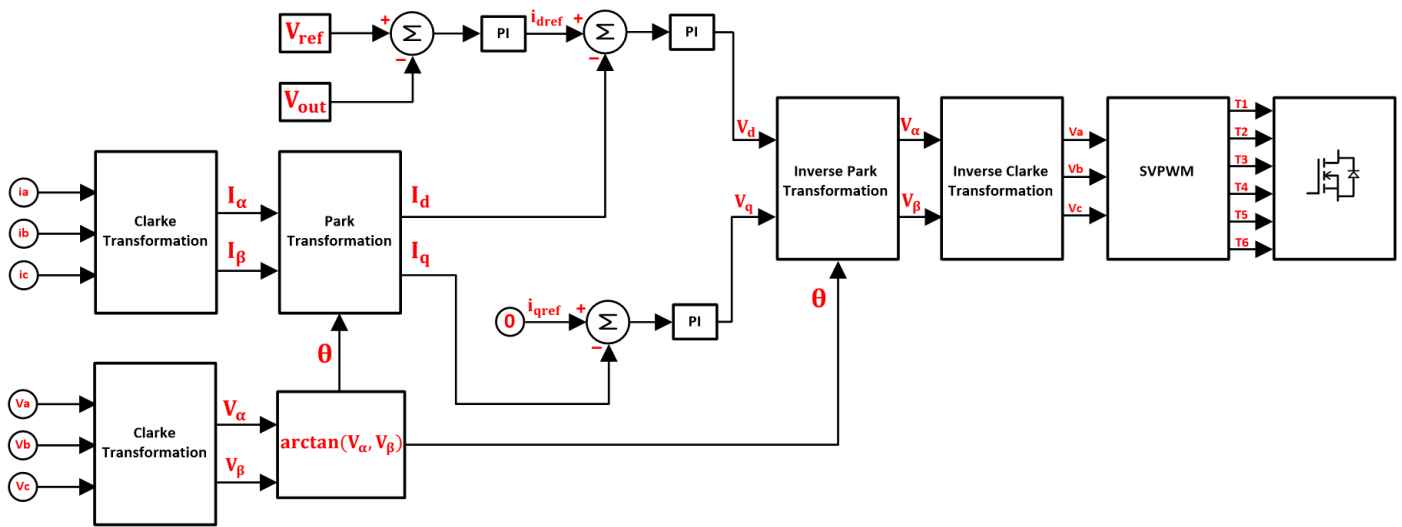

Figure 4. Control structure of 3-phase AFE converter.

Initially, phase voltages (v_a, v_b, v_c) are measured in the voltage loop followed by the calculation of α and β components (V_α, V_β) of the voltages by utilizing Clarke Transformation. Rotation angle (θ) in vector space, which is essential for the current loop, is obtained by the decomposition of the V_α and V_β values with an analog/linear phase-locked loop (PLL) loop [19,20]. Phase currents (i_a, i_b, i_c) are also measured in the current loop, and then d and q components (I_d, I_q) of the phase currents are calculated using Clarke–Park Transformations [21].

The voltage control loop consists of two nested PI (proportional-integral) controllers where the first PI controller has the output voltage (V_{out}) and reference voltage (V_{ref}) as the input values to calculate the reference value for the d-component of the current (i_{dref}). The second PI controller of the voltage control loop accepts I_d value and the i_{dref} value to output the d-component of the voltage (V_d). In order to have a unity power factor, q-component of the grid current has to become zero; therefore, i_{qref} value, which is defined as the reference value of the q-component, has to be set to zero in the PI controller of the current loop. Hence, q-component of the voltage (V_q) is gathered at the output of the PI controller.

Once V_d and V_q values are gathered initially, V_α, V_β then v_a, v_b and v_c voltages can be calculated by utilizing Inverse Park and Inverse Clarke Transformations, respectively, so that v_a, v_b and v_c voltages can be used as inputs to the SVPWM block in order to obtain the switching signals for the AFE converter. The transformation equations used in the control system are given below [21].

Clarke Transformation:

$$I_\alpha = \frac{2}{3} \cdot I_a - \frac{1}{3} \cdot (I_b - I_c) \tag{1}$$

$$I_\beta = \frac{2}{\sqrt{3}} \cdot (I_b - I_c) \tag{2}$$

Inverse–Clarke Transformation:

$$v_a = V_\alpha \tag{3}$$

$$v_b = \frac{(-V_\alpha) + \left(\sqrt{3}\right) \cdot V_\beta}{2} \tag{4}$$

$$v_c = \frac{(-V_\alpha) - \left(\sqrt{3}\right) \cdot V_\beta}{2} \tag{5}$$

Park Transformation:

$$I_d = I_\alpha \cdot \cos(\theta) + I_\beta \cdot \sin(\theta) \tag{6}$$

$$I_q = I_\beta \cdot \cos(\theta) - I_\alpha \cdot \sin(\theta) \tag{7}$$

Inverse Park Transformation:

$$V_\alpha = V_d \cdot \cos(\theta) - V_q \cdot \sin(\theta) \tag{8}$$

$$V_\beta = V_q \cdot \cos(\theta) + V_d \cdot \sin(\theta) \tag{9}$$

The expressions of the *d* and *q* components of the input voltage and current in the time domain are given in (10) and (11), respectively (L_1: line inductance, R_1: line resistance, *w*: angular frequency).

$$L_1 \cdot \frac{di_d}{dt} = w \cdot L_1 \cdot i_q + v_d - R_1 \cdot i_d - \left| \vec{v}_d \right| \tag{10}$$

$$L_1 \cdot \frac{di_q}{dt} = -w \cdot L_1 \cdot i_d + v_q - R_1 \cdot i_q - \left| \vec{v}_q \right| \tag{11}$$

In (10) and (11), all of the components are utilized in scalar form; hence, absolute values of the voltage vectors ($\vec{v}_d$, $\vec{v}_q$) have been provided as input. The main reason why the voltage vectors are produced is to have the active and reactive components of the input currents separated so that they can be controlled individually and the input power factor value can be kept as high as possible. The *θ* angle, which is used in Park and Inverse Park Transformations, has been obtained as an outcome of the Clarke Transformation of the three-phase input voltages to determine the angular velocity of the reproduced voltage vectors on the reference frame.

The simulation circuit of the AFE converter and the corresponding parameters are given in Figure 5 and Table 1, respectively.

Table 1. Simulation parameters (AFE).

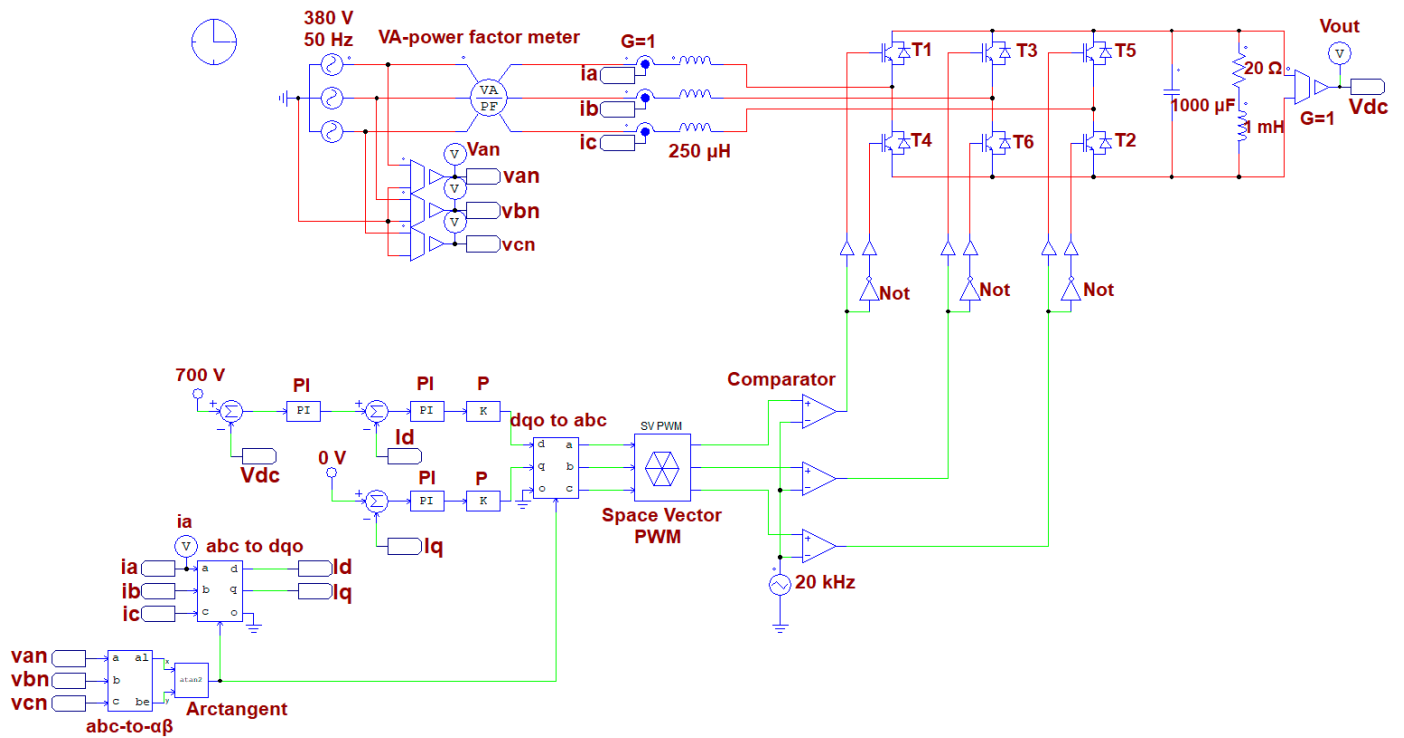| Parameters	Values
Input Voltage (V_{in})	380 V AC
Output Voltage (V_{out})	700 V
Line Frequency (f)	50 Hz
Switching Frequency (f_{sw})	20 kHz
Line Inductance (L_{in})	200 μH
Output Capacitor (C_{out})	1000 μF

Figure 5. Simulation circuit of 3-phase AFE converter.

2.2. Dual Active Bridge DC-DC Converter

The DAB converter consists of two full-bridge topologies, with an HFT positioned in the center (Figure 3). In this symmetrically structured DAB converter, the full bridge on the primary side of the HFT operates similarly to an inverter, while the full bridge on the secondary side operates as an AC-DC converter. Switch pairs (Q1–Q4, Q2–Q3) on cross arms in bridges are turned on and turned off simultaneously with a duty ratio (*D*) of 50%.

DAB converter control is implemented through the Phase Shifting Modulation (PSM) method, requiring a specific phase-shifting (ϕ) between Q1 and Q5 (as well as Q2 and Q6) switches during the conduction and cut-off periods. During this phase-shifting period, events such as power transfer, soft switching, and circuit control are performed [22].

The power transfer of the DAB converter is achieved via the leakage inductance (L_{lg}) of the HFT which is also the base parameter of the mathematical model of the circuit. Leakage inductance voltage, $v_L(t)$ is the difference between the primary $v_1(t)$ and secondary $v_2(t)$ winding voltages of the HFT which are determined according to the switching conditions. The ideal equivalent circuit of the DAB converter depending on L_{lg} is given in Figure 6 [23,24].
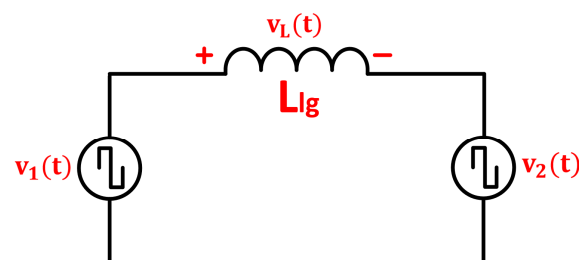

Figure 6. Ideal equivalent circuit of DAB converter.

The current waveform of the leakage inductance is needed to implement the mathematical analysis of the DAB converter. The characteristics of voltage and current waveforms

obtained according to PSM are shown in Figure 7, where two distinct operating modes have been illustrated for one switching period. The results of the detailed mathematical analysis of the operating modes are summarized in Table 2.
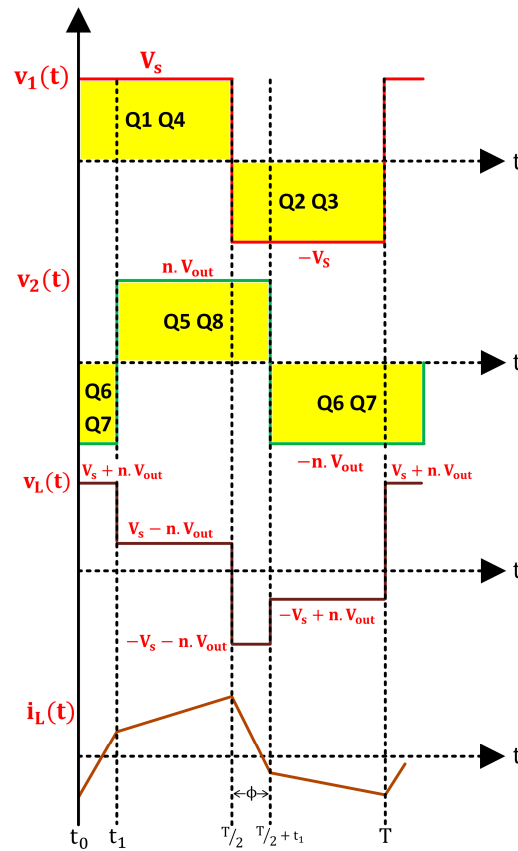

Figure 7. Characteristic current and voltage waveforms of PSM.

Table 2. Summary of results for DAB converter operating modes.

Operating Modes:	Mode-1	Mode-2
Time Interval	$t_0 < t < t_1$	$t_1 < t < T/2$
Leakage Inductance Voltage (V_L)	$V_s + n \cdot V_{out}$	$V_s - n \cdot V_{out}$
Leakage Inductance Current ($I_L(t)$)	$i_L(t_0) + \frac{(V_s + n \cdot V_{out})}{L_{lg}} \cdot t$	$i_L(t_1) + \frac{(V_s - n \cdot V_{out})}{L_{lg}} \cdot (t - t_1)$

As seen in Figure 7, the waveform of the current flowing on the leakage inductance for one switching period has a symmetrical shape; hence, the active power (P_{DAB}) transferred during this time period could be calculated utilizing Table 2.

$$P_{DAB}(t) = \frac{n \cdot V_s \cdot \phi \cdot (1 - 2 \cdot \phi)}{L_{lg} \cdot f} \tag{12}$$

The power transferred from input to output (or vice versa) is a function of the turns ratio of HFT, supply and output voltages, phase shift angle, leakage inductance value, and switching frequency. It is possible to arrange the power flow direction either from source to load or from load to source by adjusting the normalized phase shift value of ϕ, such that $(0 < \phi < 0.5)$ or $(\phi > 0.5$ or $\phi < 0)$ is selected respectively. In PSM, ϕ is the parameter that is actively controlled in order to adjust the output voltage value, as illustrated in Figure 8 with the closed-loop voltage control system.
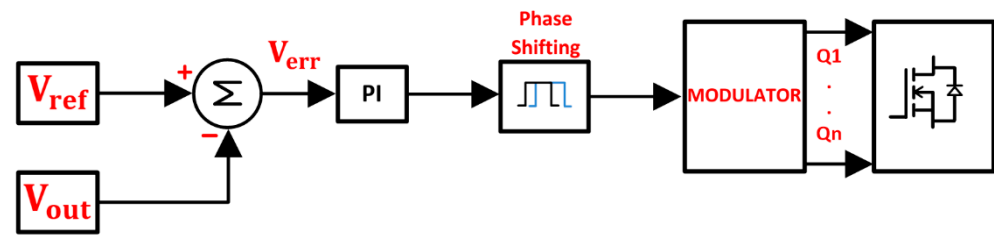
Figure 8. Control structure of DAB converter.

The simulation circuit of the DAB converter and the corresponding parameters are given in Figure 9 and Table 3, respectively.
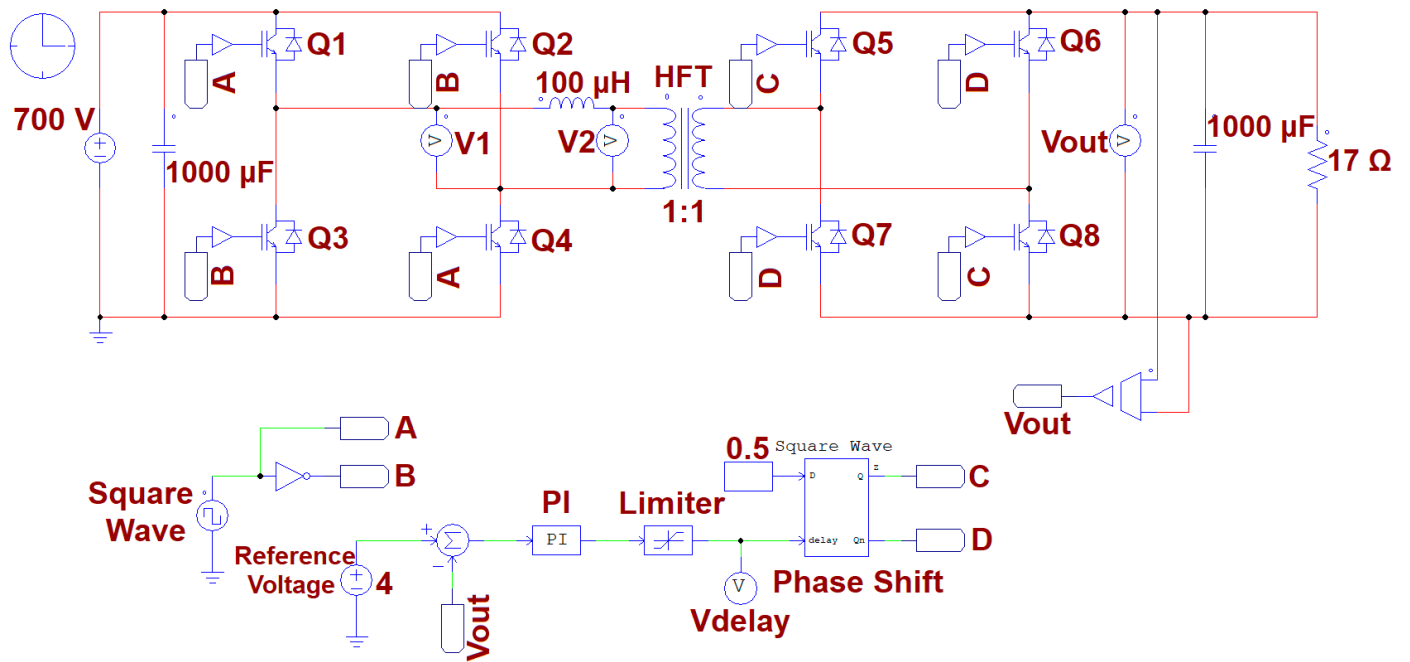

Figure 9. Simulation circuit of DAB converter.

Table 3. Simulation parameters (DAB).

Parameters	Values
Input Voltage (V_{in})	700 V
Output Voltage (V_{out})	400 V
Switching Frequency (f)	20 kHz
Input Capacitor	1000 μF
Output Capacitor	1000 μF
Leakage Inductance (L_{lg})	100 μH
Turn Ratio (n)	1

2.3. Three-Phase DC-AC Inverter

The DC-AC stage of the SST has been built with a two-level, three-phase inverter topology as shown in Figure 3, with which the SVPWM control scheme has been implemented. The SVPWM control scheme is based on the rotation of a reference vector in $\alpha\beta$ reference frame with a predefined angular velocity. Implementation of PWM generation at the output of the inverter depends on the sinusoidal three-phase voltages and the average voltage to track these sinusoidal voltages by generating minimum harmonics.

In a two-level, three-phase inverter, there are $2^3 = 8$ different applicable switching states, which can be illustrated using mechanical switches (MS). Switching states (S_A, S_B, S_C)

of the MS is determined according to the position of the MS such that either "1" or "0" position can be implemented. If "1" position is selected, then the output phase voltage is connected to (V_{DC}). Provided that "0" position is selected, the output phase voltage becomes zero (GND).

$$S_{A,B,C} = \begin{cases} 1, & V_{DC} \\ 0, & GND \end{cases} \tag{13}$$

The control method for generating space vector voltages in a three-phase inverter involves selecting appropriate switching states to create desired voltage vectors. By applying the volt-second balance principle, these vectors produce sinusoidal currents in the three phases. The inverter transitions between switching states to synthesize the required output voltage. For active states ($n = 1$ to 6), the voltage vectors are proportional to $2/3 \cdot V_{DC}$ and are spaced 60 degrees apart in the complex plane, forming a hexagonal pattern. For zero states ($n = 0, 7$), the output voltage is zero. This method ensures efficient and precise control of the inverter output.

Space voltage vectors in state space are given with (14) and (15), which are used to generate three-phase sinusoidal currents at the output of the inverter with the volt-second balance principle [25].

$$\vec{v}_n = \frac{2}{3} \cdot V_{DC} \cdot e^{j(n-1)\cdot\pi/3} \qquad n = 1, 2, 3, 4, 5, 6 \tag{14}$$

$$\vec{v}_n = 0 \qquad n = 0, 7 \tag{15}$$

The simulation circuit of the two-level DC-AC inverter with the SVPWM control scheme is given in Figure 10, and the corresponding simulation parameters are provided in Table 4.
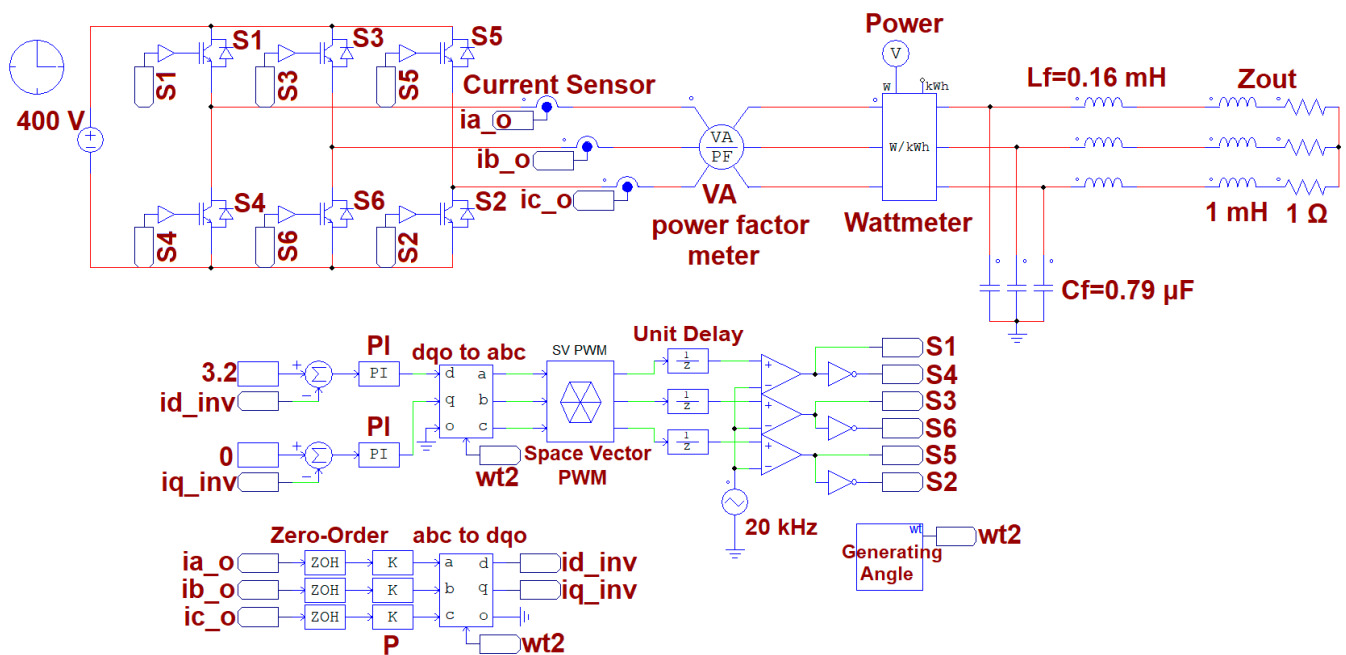

Figure 10. Simulation circuit of 3-phase DC-AC inverter.

Table 4. Simulation parameters (inverter).

Parameters	Values
Input Voltage (V_{in})	400 V
Output Voltage (V_{out})	190 V AC
Switching Frequency (f)	20 kHz
Input Capacitor (C_{in})	1000 μF
Output Filter Capacitor (C_f)	0.79 μF
Output Filter Inductor (L_f)	0.16 mH

3. Detailed Analysis of the Control Structure of the SST

3.1. Mathematical Analysis of the Control System for AFE Converter

In order to implement state space control of the AFE converter, which depends directly on the d and q components ($\vec{v}_d$ and $\vec{v}_q$) of the input three-phase voltage vectors, d and q components of the current drawn from the source should be acquired and controlled independently, as seen in (10) and (11).

First of all, reference amplitude values of the voltage vectors are determined based on Equation (16) and (17) so that $i_d(s)$ and $i_q(s)$ values could be achieved. Hence, voltage vectors depending on PI coefficients could be obtained, as seen in (18) and (19).

$$\left|\vec{v}_d\right|^* = L_1 \cdot \frac{di_d}{dt} + R_1 \cdot i_d \Rightarrow i_d(s) = \frac{1}{s \cdot L_1 + R_1} \cdot \left|\vec{v}_d\right|^* \tag{16}$$

$$\left|\vec{v}_q\right|^* = L_1 \cdot \frac{di_q}{dt} + R_1 \cdot i_q \Rightarrow i_q(s) = \frac{1}{s \cdot L_1 + R_1} \cdot \left|\vec{v}_q\right|^* \tag{17}$$

In this case, voltage vectors can be rewritten based on the PI coefficients.

$$\left|\vec{v}_d\right| = v_d + w \cdot L_1 \cdot i_q - \left(K_p + \frac{K_i}{s}\right) \cdot (i_d^* - i_d) \tag{18}$$

$$\left|\vec{v}_q\right| = v_q + w \cdot L_1 \cdot i_d - \left(K_p + \frac{K_i}{s}\right) \cdot (i_q^* - i_q) \tag{19}$$

By substituting (18) and (19) in (10) and (11), respectively, i_d and i_q components can be decoupled so that closed-loop current and voltage control can be implemented [26,27]

3.1.1. Development of the Voltage Control Loop for the AFE Converter

The voltage control loop is used for setting the output voltage level at a desired level and for determining the reference value of the d component of the current (i_{dref}). The transfer function of the output voltage acquired with the help of the voltage loop is given in (20), where C_1 is the output capacitor of the converter, T_s is the sampling period, K_{AFE} and T_{AFE} parameters are proportional and time-constant components of the PI controller.

$$\frac{V_{C1}(s)}{V_{C1}^*(s)} = \frac{1}{1 + \left[C_1 \cdot T_{AFE} \cdot s^2 \cdot \frac{(1 + 3 \cdot T_s \cdot s)}{0.75 \cdot K_{AFE} \cdot (T_{AFE} \cdot s + 1)}\right]} \tag{20}$$

3.1.2. Development of the Current Control Loop for the AFE Converter

The current control loop can be designed simultaneously for i_d and i_q components of the input current though only the design details of i_d will be provided. Prior to specifying the closed-loop transfer function of the current loop, it is essential to define some of the parameters, which are the gain of the converter (G) and the ratio of the proportional

coefficient to the integration coefficient defined as τ coefficient. Generalized transfer function of the i_d current is given in (21).

$$\frac{i_d(s)}{i_d^*(s)} = \frac{1}{\left(\frac{1.5 \cdot T_s \cdot R_1 \cdot \tau}{K_{AFE} \cdot G}\right) \cdot s^2 + \left(\frac{R_1 \cdot \tau}{K_{AFE} \cdot G}\right) \cdot s + 1} \tag{21}$$

3.2. Mathematical Analysis of the Control System for DAB Converter

There are two distinct DAB converter closed-loop control systems designed one of which is the voltage control loop for keeping the output voltage within the desired limits. The voltage control signal acquired as a result of this control loop is utilized as a reference value for the closed-loop current control [28–30].

3.2.1. Development of the Voltage Control Loop for the DAB Converter

The transfer function of the voltage loop covers the proportional coefficient K_{DAB}, integration coefficient K_{I1}, the output voltage value V_{C2}, the output capacitance value C_2, and the output impedance value Z_{out}.

$$\frac{V_{C2}(s)}{V_{C2}^*(s)} = \frac{\left(-\frac{K_{I1}}{2 \cdot C_2 \cdot L_{lg} \cdot f}\right)}{s^2 + \left(\frac{K_{DAB}}{2 \cdot C_2 \cdot L_{lg} \cdot f} + \frac{1}{C_2 \cdot Z_{out}}\right) \cdot s - \frac{K_{I1}}{2 \cdot C_2 \cdot L_{lg} \cdot f}} \tag{22}$$

3.2.2. Development of the Current Control Loop for the DAB Converter

Input current of DAB converter (I_{tr1}) is kept at a certain average level by the current loop in order to limit the current stress on the semiconductor devices constructing the DAB stage. The reference current value of the input current (I_{tr1}^*) is determined by utilizing the transfer function of the voltage loop.

$$\frac{I_{tr1}(s)}{I_{tr1}^*(s)} = \frac{1}{1 + \left(\frac{V_{C2} \cdot (1 - 2 \cdot D)}{2 \cdot n \cdot f \cdot L_{lg}}\right) \cdot s} \tag{23}$$

3.3. Mathematical Analysis of the Control System for Inverter

The input voltage of the inverter circuit is essentially provided from the output of the DAB converter; therefore, this should be taken into consideration when designing current and voltage loops [31,32].

3.3.1. Development of the Voltage Control Loop for the Inverter

The transfer function of the control loop to determine the output voltage of the SST contains the proportional coefficient K_{inv}, integration coefficient K_{I2}, output filter inductance L_f and capacitance C_f as provided in (24).

$$\frac{V_{out}(s)}{V_{out}^*(s)} = \frac{K_{inv} \cdot s + K_{I2}}{L_f \cdot C_f \cdot s^3 + C_f \cdot K_{inv} \cdot s^2 + (K_{inv} \cdot K_{I2} + 1) \cdot s + K_{inv} \cdot K_{I2}} \tag{24}$$

3.3.2. Development of the Current Control Loop for the Inverter

The output filter of a three-phase inverter consists of inductors (L_f) connected in series on each phase and capacitors (C_f) connected in a star configuration designed to attenuate high-frequency harmonics and stabilize the AC output. The precise values of L_f and C_f are critical for properly tuning the control loop and optimizing the dynamic response and harmonic attenuation of the system. The output current (I_{out}) of the SST is directly regulated by the current loop of the inverter circuit, while the C_f plays a crucial role in minimizing the total THD of I_{out}. Under the condition of constant input voltage (V_{C2}), input

current (I_{tr2}) of the inverter is controlled; however, the value of I_{tr2} is also the outcome of the PWM signal states produced by the space vector control algorithm, as shown in (25).

$$\frac{I_{tr2}(s)}{I^*_{tr2}(s)} \propto f(S_{A,B,C}) \tag{25}$$

The transfer function of the I_{out} provided in (26), covers the time constant of the controller T_{inv}, values of output filter components R_f and L_f.

$$\frac{I_{out}(s)}{I^*_{out}(s)} = \frac{K_{inv} \cdot (1 + T_{inv} \cdot s) \cdot C_f}{L_f \cdot C_f \cdot s^2 + R_f \cdot C_f \cdot s + 1} \tag{26}$$

4. Simulation of a 10 kVA AC-AC Conversion System Built with 3-Stage SST

In this section, simulation results of the proposed linear-based control system for a 10 kVA SST using the electrical parameters given in Tables 1–3 have been presented. Although the control system of SST is complex, individual current and voltage loops are designed for each topology (AC-DC, DC-DC, DC-AC) that constitutes SST in the simulation; hence, the control system becomes simpler. While the interaction within the voltage loops is determined by the DC link capacitor voltages (V_{C1}, V_{C2}), the feedback within the current loops is processed through the amount of current transferred (I_{tr1}, I_{tr2}) between each stage. The general structure of the proposed linear-based control system is given in Figure 11.
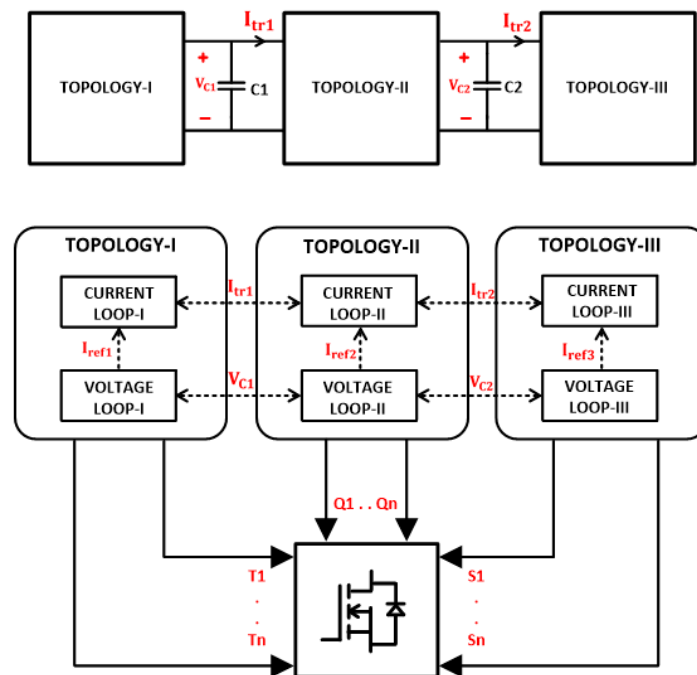

Figure 11. The general structure of the proposed linear-based control system for SST.

The SST simulation circuit covering each power stage with the control systems mentioned above is illustrated in Figure 12, and the assessment of the circuit performance based on the simulation results is provided below. It should be noted that the simulation circuits given for DAB (Figure 9) and Inverter (Figure 10) are actually controlled independently and consist of only the voltage loop. However, there are dependent voltage and current loops for each topology that constitute the SST from the proposed linear-based control system.
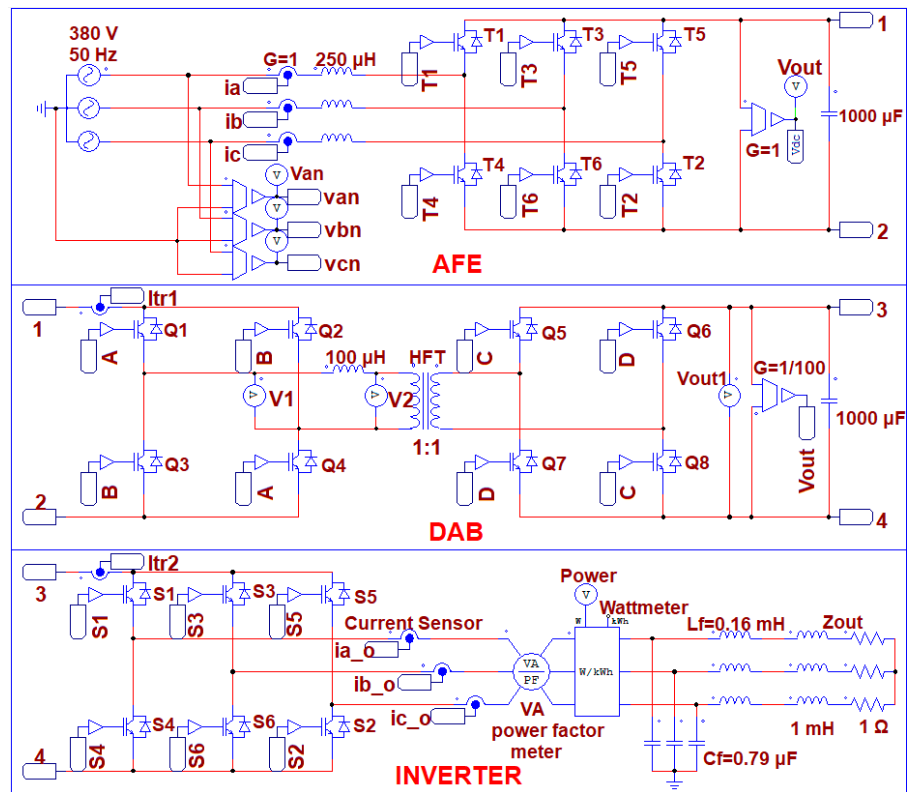
(**a**)
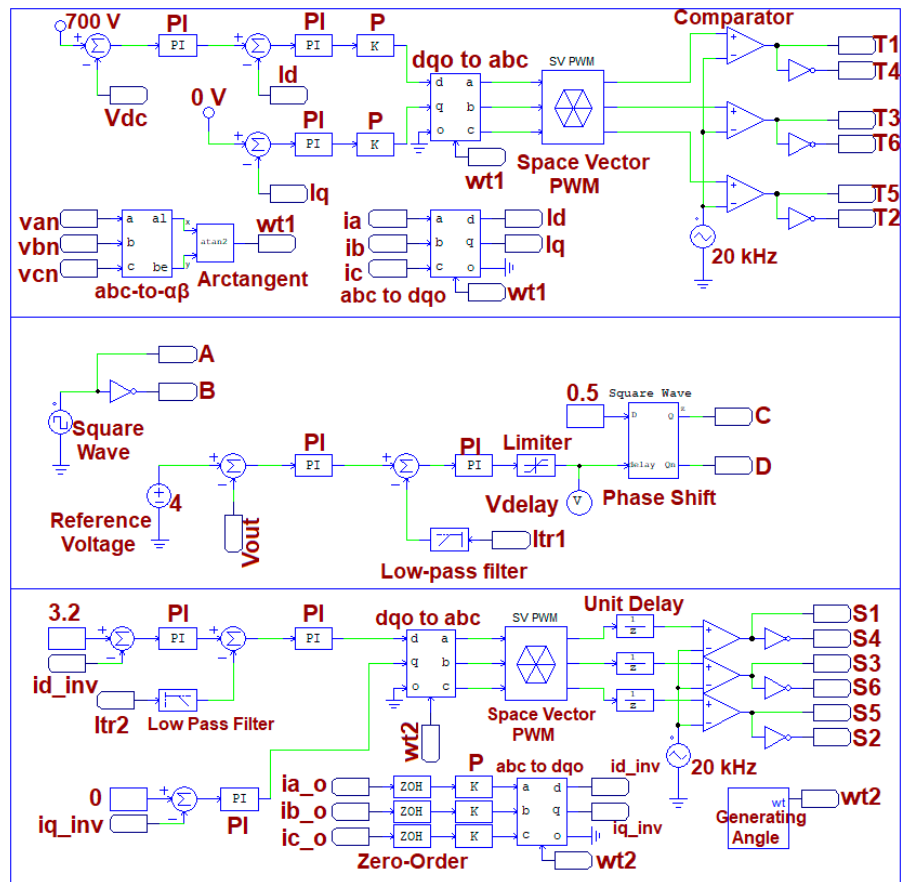
(**b**)

Figure 12. Simulation circuit of SST (**a**) power stage, (**b**) control stage.

In the AC-DC converter stage, the utilization of the SVPWM technique enables the power factor to achieve approximately 0.99 without the need for any additional component under inductive load. Additionally, the transient state of the input current on the three-phase grid side lasts for an average of 20 ms (Figure 13), after which the output voltage of the AC-DC converter stabilizes and remains constant at 700 V. Since the voltage increase in the transient region reaches approximately 735 V at most, the performance of the closed-loop control system is considered successful (Figure 14).
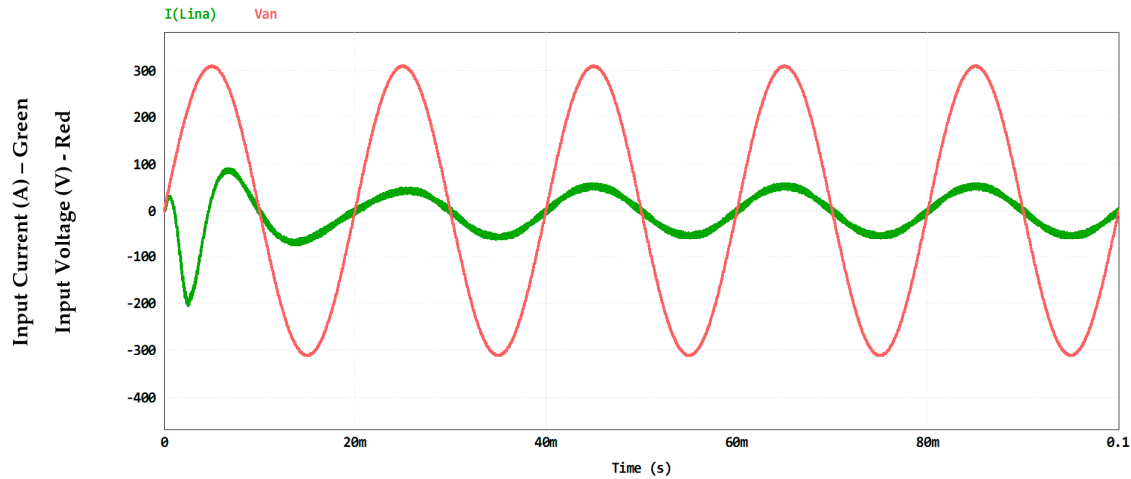

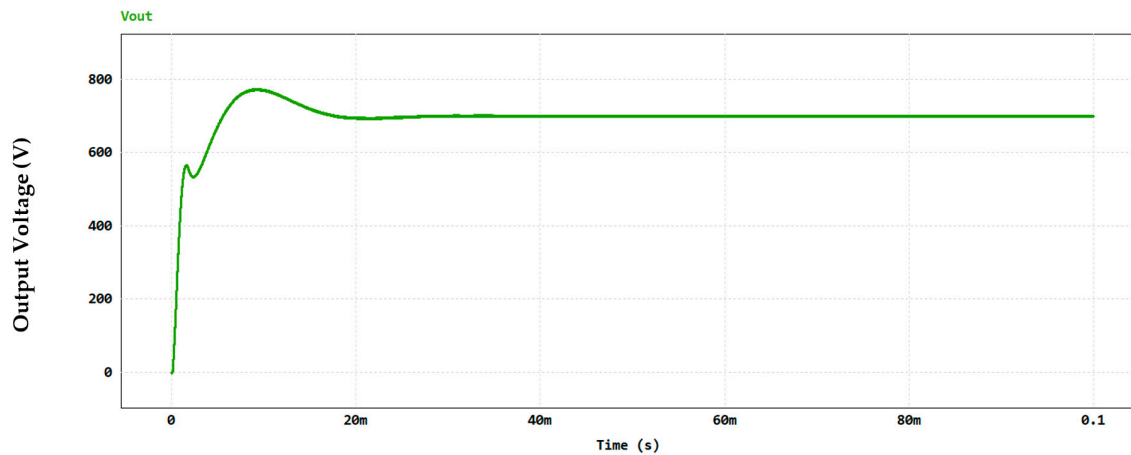**Figure 13.** Input current and voltage waveforms of 3-phase AC-DC converter.

Figure 14. Output voltage waveform of 3-phase AC-DC converter.

Figure 15 illustrates the waveforms of the primary winding voltage V_1, secondary winding voltage V_2, and the current $I(L1)$ flowing through the leakage inductance in the DAB DC-DC converter. Additionally, the waveform of the output voltage from the DAB converter is illustrated in Figure 16, reaching its peak value of 437 V within 17 ms and subsequently stabilizing to the desired voltage level of 400 V in 40 ms. Even though a voltage overshoot occurs at the output stage, it is observed that the dynamic response of the DAB closed-loop control system is quite fast.
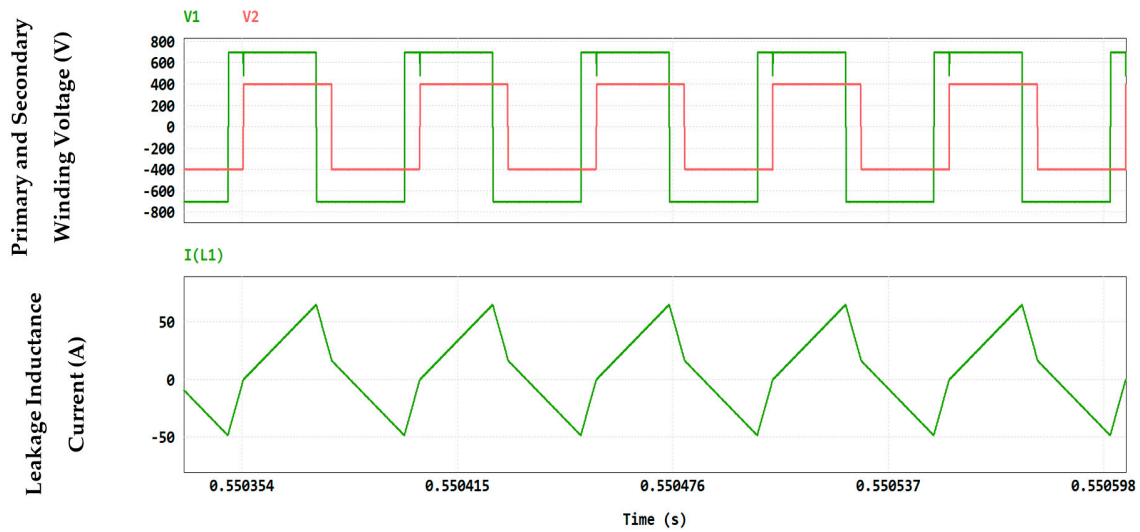
Figure 15. Primary winding voltage V1, secondary winding voltage V2 and leakage inductance current I (L1) waveforms.
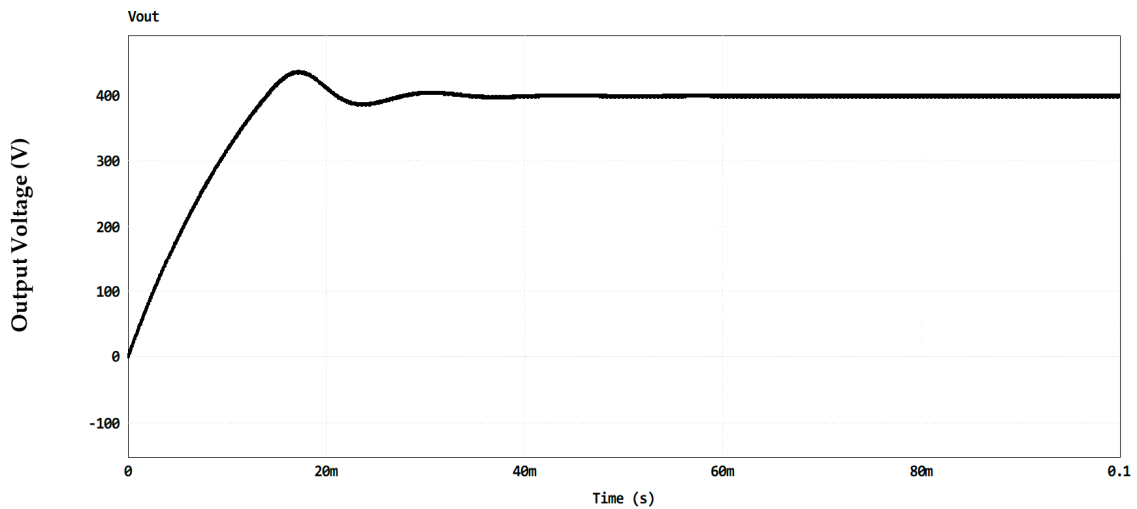

Figure 16. Output voltage waveform of DAB converter.

As illustrated in Figure 15, the phase difference between the primary and secondary winding voltages in the HFT indicates the successful implementation of PSM. This phase difference is optimally determined in the time domain through the proposed control method, with the phase-shifting value between the primary and secondary voltages being approximately 4 μs.

This phase shift is a critical parameter for ensuring efficient system operation and demonstrates the accuracy and effectiveness of the proposed control method. The determination of the optimal phase shift value is crucial for enhancing both system stability and performance. Proper adjustment of the phase difference allows for maximum efficiency in power transfer, significantly contributing to overall system efficiency.

Moreover, due to the linear-based nature of the proposed control method, the phase shift value can be precisely adjusted and continuously monitored. This capability enables the system to respond rapidly to changes in system dynamics and load variations. Thus, the results clearly illustrate the superior performance and advantages of the proposed control method in optimizing the phase-shifting mechanism within the HFT.

The PSM technique used in the DAB converter allows soft switching of the semiconductor devices so that each of the switches on the output bridge can switch under

zero voltage conditions. The current and voltage waveforms of the Q5 switch, shown in Figure 17, illustrate that soft switching is achieved.
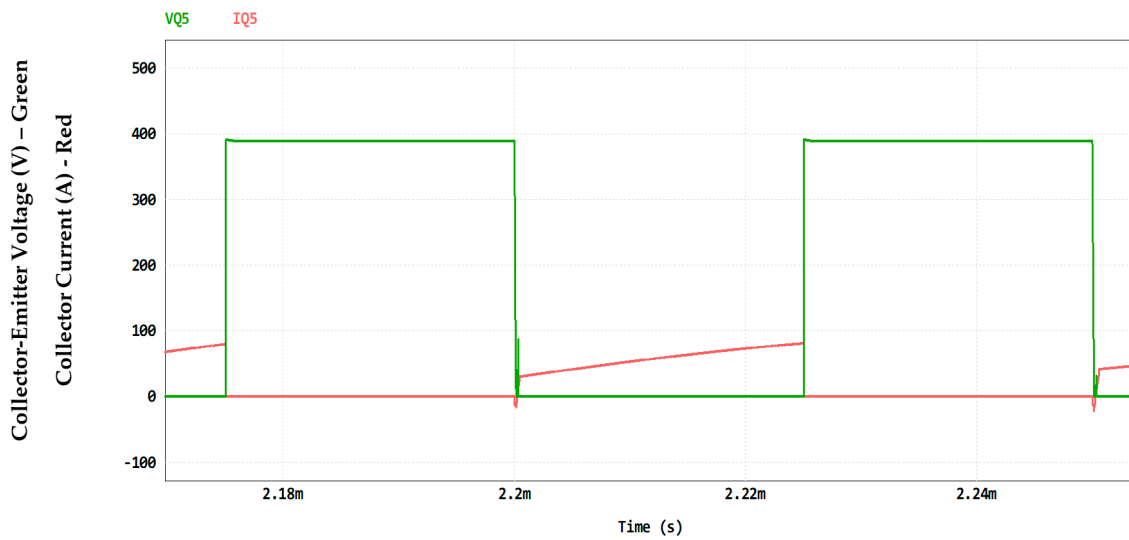

Figure 17. Current and voltage waveforms of the Q5.

Based on the simulation results of the control system, output current and voltage can reach the set value in 40 ms. Although the THD value increases in the transient region, there is no significant change in the peak points of AC current/voltage levels. On the other hand, it is observed that the THD value for the output current of the SST remains within the maximum range of 4.20%, indicating that the proposed control method operates effectively with good performance (Figure 18).
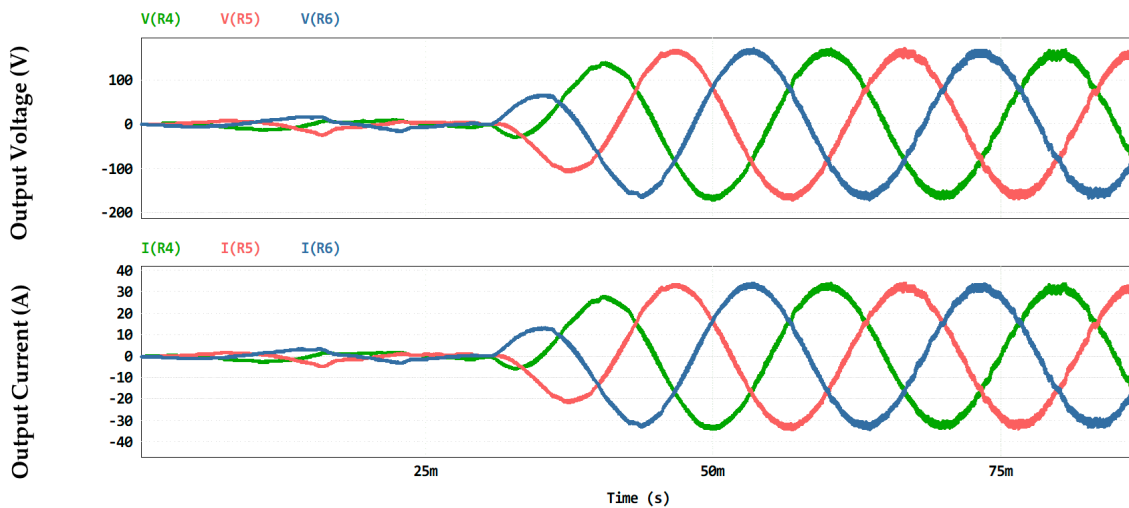

Figure 18. Output voltage and current waveforms of SST.

One of the advantageous features of SST is its capability to allow bidirectional power flow. In order to provide reverse power flow, the phase shift value of the DAB converter and the reference i_{dref} used in the control of the DC-AC inverter must be adjusted appropriately. The most effective way to demonstrate bidirectional power flow in SST is by connecting the output inverter to a three-phase voltage source instead of a static three-phase load, allowing the input AFE stage of SST to serve as the output stage for reverse power flow through the adjustment of appropriate ϕ and i_{dref} values (Figure 19).
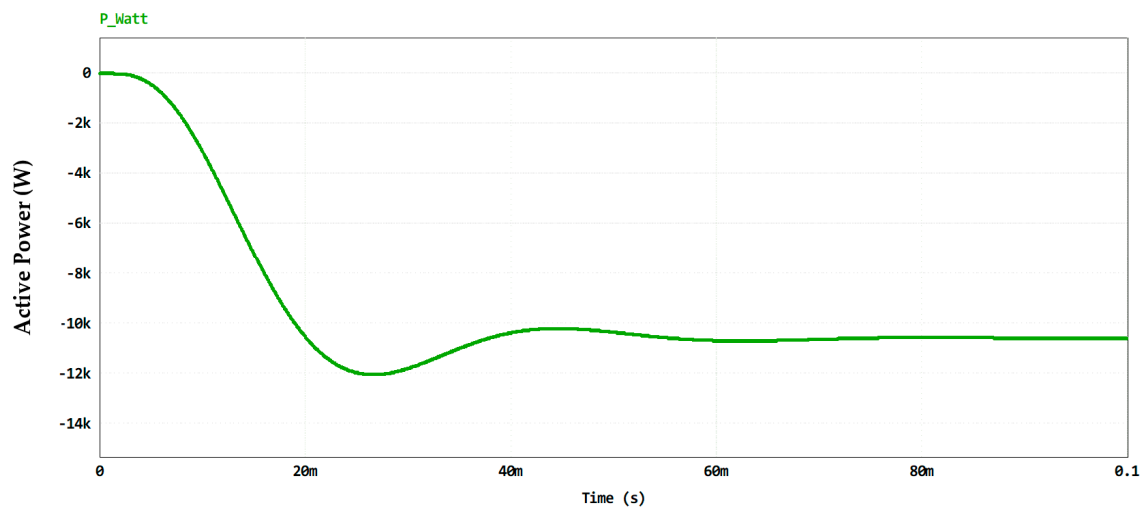
Figure 19. Active power flow in the opposite direction depending on ϕ and i_{dref}.

Finally, the dynamic response of the Solid-State Transformer (SST) is expected to be exceptionally fast under various output loads and corresponding output currents. This rapid response is particularly critical in applications where load conditions can change abruptly. When the inverter stage operates as a current source, the system's ability to swiftly adjust the output current value in response to varying load conditions is significantly enhanced.

The key mechanism facilitating this rapid adjustment is the direct control of the current i_d, as depicted in Figure 20. By manipulating the i_d value, the SST can precisely increase or decrease the output current to match the changing demands of the load. This direct control approach allows for a highly responsive system, ensuring that the SST can maintain optimal performance and stability even under dynamic and fluctuating load conditions.
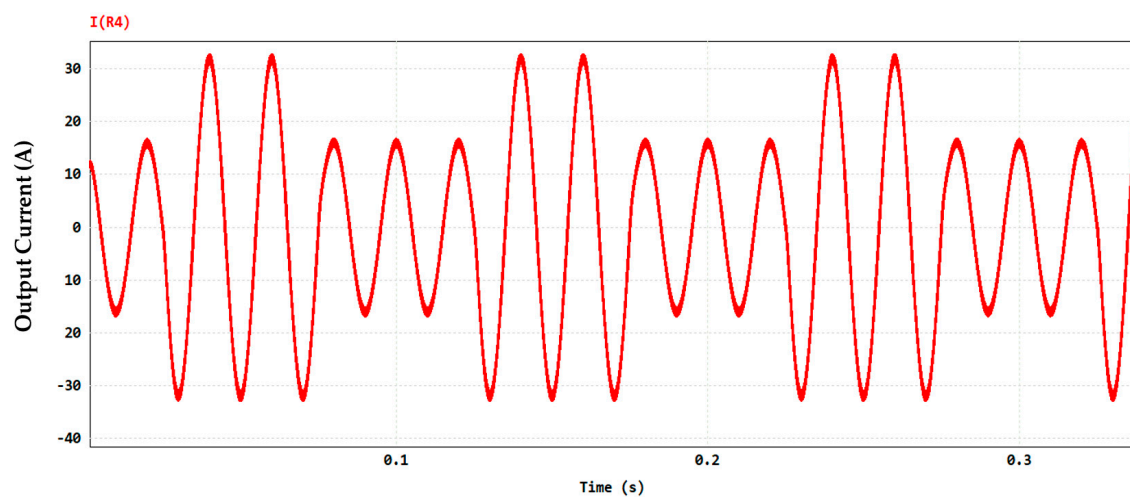

Figure 20. Dynamic response of SST to output load changes.

Furthermore, the implementation of the current source operation in the inverter stage provides several technical advantages. It allows for better regulation of output currents, minimizing transient effects that can occur during sudden load changes. This not only improves the overall efficiency of the SST but also contributes to the longevity and reliability of the system by reducing stress on the components.

The IGBTs in the SST are switched at an average frequency of 20 kHz. Since this switching frequency is not exceedingly high, significant noise issues are not anticipated in the SST. Furthermore, with the selection of appropriate SiC-based IGBT [33] switches

and a well-designed HFT [34], it is expected that the SST's operating temperature will be maintained at desired levels through either passive or active cooling methods [35].

In the experimental testing of this control method, a total of six loops—three for current and three for voltage—need to be operated. Additionally, in the control system of any converter, a signal obtained from the output of one loop serves as the input information for another loop. As a result, some delays may occur during the experimental implementation of the proposed control method. However, these delays occur over very short time intervals, and modern DSP (Digital Signal Processing) and (Field-Programmable Gate Array) modules are capable of executing such linear-based closed-loop control systems very quickly [36].

Through extensive simulation studies, the proposed control system demonstrated a significant enhancement in the overall efficiency of SSTs, achieving approximately 96%. In the efficiency calculation, the losses of the IGBT switches in each converter of the SST were determined using the Level-2 Model [37,38]. These calculations were performed using the IGBT parameters provided in Table 5. Additionally, loss calculations for the magnetic components were conducted, but only for the DAB converter. This is because the magnetic component losses in the AFE and inverter are negligible compared to the switch losses. These results validate the effectiveness of the proposed system, highlighting its potential to improve SST performance in practical applications.

Table 5. IGBT parameters used in the switching loss calculation according to the Level-2 model.

CONVERTER	V_{CE}	$V_{GE(th)}$	g_{fs}	t_f	C_{ies}	C_{oes}	R_{CEon}	R_G
AFE DAB (Primary)	900 V	2.1 V	8.7 S	4 ns	410 pF	45 pF	120 mΩ	12 Ω
DAB (Seconder) Inverter	650 V	2.2 V	4.9 S	8 ns	640 pF	45 pF	120 mΩ	6 Ω

V_{CE}: Maximum Collector-Emitter Voltage, $V_{GE(th)}$: Gate Threshold Voltage, g_{fs}: Transconductance, t_f: Fall Time, C_{ies}: Input Capacitance, C_{oes}: Output Capacitance, R_{CEon}: Collector-Emitter on Resistance, R_G: Internal Gate Resistance.

5. Conclusions

In this study, a 10 kVA SST system with a new linear-based closed-loop control system has been designed by implementing individual closed-loop voltage and current control stages for each power converter topology. In order to cope with the communication between each power stage along with the identification of the reference values, the current flowing between each power stage and the voltage across the interconnecting DC link capacitors have been measured.

In order to evaluate the performance of the proposed control method, a general simulation study has been implemented based on which power factor correction, soft switching, and bidirectional power flow features have been achieved. Additionally, for various output load conditions, the control system was found to have good dynamic response along with good THD performance as low as 5%.

The proposed control method has several significant advantages compared to traditional methods. Firstly, its linear-based structure offers a simpler and more comprehensible control strategy. Additionally, the closed-loop control system continuously monitors the system's performance through feedback mechanisms and makes immediate corrections, which enhances overall system efficiency.

As a result, the proposed control method offers significant advantages by enabling the SST to operate at high performance levels. Nonetheless, its certain limitations and potential drawbacks should be considered, and appropriate measures should be taken. If implemented and optimized correctly, this new control system can lead to substantial improvements in SST performance.

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